ICPT International Conference on Planarization/CMP Technology

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ICPT 2025 - INTERNATIONAL CONFERENCE ON PLANARIZATION/CMP TECHNOLOGY

TUTORIAL

TUTORIALS

October 29, 2025

OCTOBER 29, 2025 Wednesday

08:00-09:00	**Registration**
09:00-09:10	**Opening Remarks** Tutorial Chair Baoguo Zhang Hebei University of Technology
Session Chair : Baoguo Zhang	
09:10-10:10	**FinFET CMP Process Technology and Challenges** Gary Lam Applied Materials
10:10-10:30	**Coffee Break**
10:30-11:30	**CMP for More-than-Moore** Gerfried Zwicker Fraunhofer Institute
11:30-12:30	**Fundamentals of CMP Chemistry** Kangchun Lee Kwangwoon University
12:30-13:30	**Lunch Break**

Session Chair : Yuchun Wang	
13:30-14:30	**Inside CMP: Material Removal Mechanisms Empowered by CMP Pad Conditioning** Yongsik Moon EHWA Diamond
14:30-15:30	**Post CMP Cleaner Development** Don Frye Entegris
15:30-15:50	**Coffee Break**
15:50-16:50	**Metrology and Inspection for Heterogeneous Integration** Taegon Kim Hanyang University
16:50-17:00	**Closing Remarks** Tutorial Chair Baoguo Zhang Hebei University of Technology
17:00-18:00	**Registration**

TUTORIAL BIO INFORMATIONT

TUTORIAL

Gary Lam

Applied Materials

FinFET CMP Process Technology and Challenges

Gary Lam is a CMP Technical Program Director at Applied Materials in Sunnyvale, USA. He earned a B.S. degree in Mechanical Engineering from U.C. Berkeley in 1998. With over 25 years in the CMP Division at Applied Materials, he began in Cu CMP process engineering and development. In 2005, he moved to a Customer Account Technologist role, qualifying new CMP platforms and processes for logic and memory fabs across North America, Asia, and Europe. Recently, he has taken on a new role focused on driving product improvement programs for next-generation CMP technologies.

Gerfried Zwicker

Fraunhofer Institute

CMP for More-than-Moore

Gerfried Zwicker earned his PhD for his research on ZnO surface properties at the Fritz-Haber-Institute in Berlin. He joined Fraunhofer Institute for Microstructure Technology IMT in 1985, working on CMOS technology using x-ray lithography, focusing on reactive ion etching. After moving to Fraunhofer Institute for Silicon Technology ISIT in Itzehoe in 1995, he focused on CMP, responsible for CMP tool development, consumables evaluation, and process adoption for MEMS and powerMOS applications. Dr. Gerfried Zwicker is the founder and organizer of the European CMP Users Meeting and was a co-founder and member of the Executive Committee of ICPT. He is the author/co-author of more than 50 publications and book contributions.

Kangchun Lee

Kwangwoon University

Fundamentals of CMP Chemistry

Kangchun Lee received a Ph.D. in Energy Engineering and a B.S. in Materials Science and Engineering from Hanyang University in Seoul, Republic of Korea, respectively. He currently serves as a Topical Advisory Panel Member in Applied Sciences and an Early Career Scholars Member in material science for the journal of Materials Research. His research focuses on Advanced CMP/Post-Cleaning Processes and cutting-edge materials based on Colloid- and Electrochemistry. He was a Staff Engineer at the Semiconductor R&D Center of Samsung Electronics from 2020 to 2023, where he participated in the development and mass production transfer of the GAAFET-based sub-3nm foundry CMP process and integration.

Yongsik Moon

EHWA Diamond

Inside CMP: Material Removal Mechanisms Empowered by CMP Pad Conditioning

Yongsik Moon is currently the Director of Technology in the CMP Disk Business Unit at EHWA Diamond, Korea, with over 20 years of experience in CMP across equipment makers, IDMs, logic foundries, and memory semiconductor companies. He began his CMP career in 2000 as a CMP Process Development Engineer at Applied Materials, where he developed Best Known Method (BKM) recipes for Cu interconnect CMP that remain in use today. He is also a co-author of the book "Advances in Chemical Mechanical Planarization", edited by Prof. Suryadevara Babu (Elsevier, 2016). His diverse career offers a unique, end-to-end view of CMP, from R&D to advanced manufacturing and data-driven innovation.

Don Frye

Entegris, Inc

Post CMP Cleaner Development

Don Frye has worked at Entegris for 11 years in developing new post-CMP cleaners and has published several papers at ICPT and other conferences. He managed the Post CMP program and directed the cleaner projects during this time. He worked for 5 years at Henkel, developing new advanced underfills, low-temperature sintered silver adhesives, and wafer coatings. While at Henkel, Don was a Sr. Development and Sr. Research Scientist. He worked across several areas, developing new materials and processes for Wafer dielectrics and Packaging dielectrics.

Taegon Kim

Hanyang University

Metrology and Inspection for Heterogeneous Integration

Tae-Gon Kim is a faculty member in the Department of Smart Convergence Engineering at Hanyang University ERICA. Throughout his distinguished research career, he has established himself as a leading expert in semiconductor cleaning and chemical mechanical polishing technologies. His pioneering work encompasses advanced thin film characterization, in-line metrology techniques for cutting-edge technology nodes, and the development of in-line 3D-AFM technology for three-dimensional nanostructure analysis particularly for sidewall characterization of FinFET and nanowire architectures.

FINFET CMP PROCESS TECHNOLOGY AND CHALLENGES

Gary Lam

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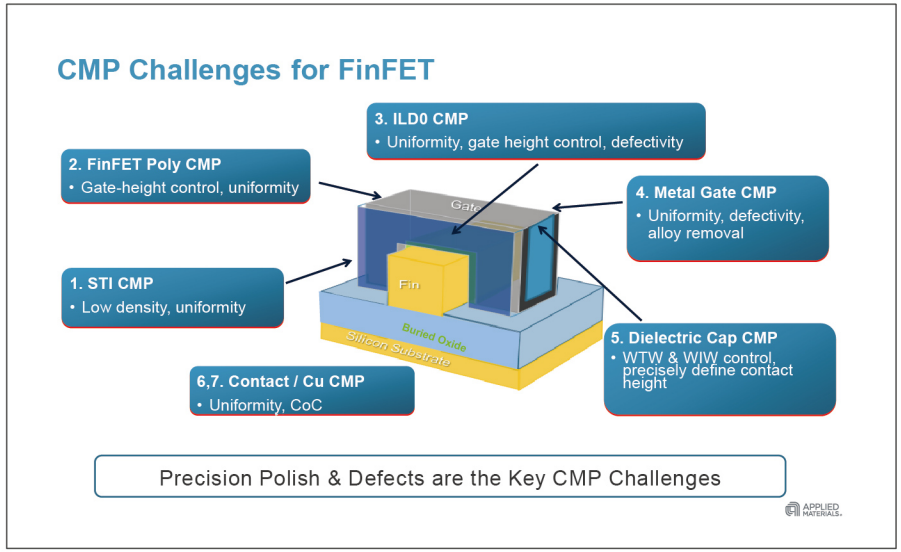
As device dimension continues to shrink in scale, CMP plays a critical role in the enabling of FinFET technology performance. In order to achieve device performance requirement, advance CMP technology solutions are applied to address the challenges in Front-End CMP, Replacement Gate CMP, and Back-End CMP processes.

FinFET transistor formation requires precise Gate Height Control during Front-End CMP and Replacement Gate CMP. Advanced CMP Polish Head is needed to control CMP removal profile across the wafer to achieve Within-Wafer and Wafer-to-Wafer planarization and uniformity performance requirement. Advanced CMP Optical Endpoint Process Control is used in combination with advanced CMP Polish Head to further improve post CMP thickness control and uniformity performance.

FinFET yield performance requires low defect level after each CMP step. Major defects induced by CMP are surface particles and scratch defects. To achieve low surface particle defect level, Cleaner with chemistry buffing and brush scrubbing are key critical steps during CMP Cleaning. To achieve low scratch defect level, process recipe design using low pressure polish and polish pad cleaning hardware can be applied.



CMP Process Steps Challenges

CMP FOR MORE-THAN-MOORE

Gerfried Zwicker

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More-than-Moore applications like MEMS, analog, powerMOS, optoMEMS, packaging, bonding etc. require smooth and even surfaces which can only be achieved by chemical-mechanical polishing CMP. Due to increasing mass fabrication of these devices multiple CMP processes must fulfill the same specifications as those for microelectronics manufacturing. After a short summary of MEMS manufacturing technologies several typical examples of the application of CMP processes for making sensors, actuators, optoMEMS, powerMOS, and for hybrid bonding of microsystems and chip thinning for failure analysis will be discussed.

FUNDAMENTALS OF CMP CHEMISTRY

Kangchun Lee

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Chemical Mechanical Planarization (CMP) has become a cornerstone process in advanced semiconductor manufacturing, enabling the realization of increasingly complex device architectures. Its success relies on a delicate balance of chemical reactions and mechanical interactions that together achieve global surface flatness and controlled material removal, both of which are essential for device functionality, performance, and long-term reliability. This tutorial will first provide a systematic overview of the fundamental chemistry underlying CMP, with particular focus on the design and function of slurry components such as abrasives, oxidizers, complexing agents, and corrosion inhibitors. By examining the interplay between these components at the wafer-slurry interface, the session will highlight how they govern removal rates, selectivity, defectivity, and overall process stability. Building upon this foundation, the tutorial will explore the translation of chemical principles into practical applications, including optimized slurry formulations and process strategies for logic and memory integration.

A special emphasis will be placed on the rapidly emerging Cu Hybrid Bonding CMP, which is regarded as a key enabler for three-dimensional integration and heterogeneous packaging. Despite its potential, this approach faces critical challenges such as dishing, erosion, bonding interface contamination, and reliability concerns. The tutorial will review recent advances in addressing these issues, including novel slurry chemistries, optimized process conditions, and defect mitigation strategies. By integrating both fundamental understanding and application-oriented insights, the session aims to provide participants with a comprehensive framework for appreciating the evolving role of chemistry in advancing CMP technology.

INSIDE CMP: MATERIAL REMOVAL MECHANISMS EMPOWERED BY CMP PAD CONDITIONING

Yongsik Moon

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Chemical Mechanical Polishing (CMP), introduced by Dr. Klaus Beyer at IBM in 1983, is essential to semiconductor manufacturing. As device complexity increases with finer geometries, new materials, and 3D integration, CMP requirements—particularly pad conditioning—have grown more demanding.

Pad conditioning maintains the functional surface of the polishing pad by restoring micro-asperities, preventing glazing, and controlling pad cut rate (PCR). Proper conditioning ensures stable material removal rates (MRR), uniformity (WIWNU), and low defectivity, while avoiding issues like glazing from under-conditioning or premature groove wear and defects from over-conditioning.

This tutorial reviews CMP pad conditioning fundamentals, current technologies, and future directions. It examines removal mechanisms, pad surface maintenance, and diamond-disk interactions. Conditioning typically uses diamond abrasives, whose effectiveness depends on aggressiveness, geometry, orientation, and bonding method. Manufacturing approaches include electroplating (low cost, limited durability), sintering (robust), brazing (strong retention), and advanced Chemical Vapor Deposition (CVD), which offers precise diamond placement, chemical inertness, and MRR stability for advanced nodes.

Technological progress spans both macro- and micro-scales: optimizing disk geometry, active diamond count, and cut rate; and refining diamond size, shape, orientation, and bonding to extend disk life and ensure consistent pad engagement.

Future challenges stem from hard or chemically resistant materials such as SiC, GaN, Mo, and Ru, which demand robust, precise conditioning. Next-generation conditioners must balance low PCR with sufficient roughness, minimize scratches, and extend pad and disk lifetimes. Advances will likely include AI-based diamond inspection, optimized diamond layouts, and stronger, more chemically resistant bonding materials.

In conclusion, pad conditioning remains central to CMP performance. Sustained innovation in materials, disk design, and adaptive control will be critical to enabling reliable, high-yield semiconductor manufacturing in future technology nodes.

POST CMP CLEANER DEVELOPMENT

Don Frye

Principal Scientist, Technical Program Management, Entegris, USA

1.Introduction to Post-CMP Cleaning

What is CMP?
Brief overview of Chemical Mechanical Planarization as a critical semiconductor manufacturing step.

Why is Post-CMP Cleaning Necessary?
-To remove contaminants that cause defects and yield loss.
-To prepare a pristine surface for the subsequent process step.

Goals of an Effective Post-CMP Clean:
-Complete removal of slurry abrasive particles.
-Removal of abraded wafer material and metallic contaminants.
-Removal of organic residues (e.g., from corrosion inhibitors like BTA).
-Prevention of surface damage (pitting, corrosion, scratching).
-Control of final surface topography and hydrophilicity.

2.Core Principles & Mechanisms

Contamination Sources:
-Slurry Abrasives (Silica, Ceria, Alumina).
-Planarized Material (e.g., metal fragments, dielectric dust).
-Dissolved Metallic Ions (e.g., Cu^{2+}).
-Organic Residues from slurry chemistry.

Key Cleaning Mechanisms:
-Physical Force: Brush scrubbing, megasonics, high-pressure sprays.
-Chemical Action:
  Etching/Undercutting: Slightly etching the substrate to lift off adhered particles.
  Surface Charge Modification: Using pH (e.g., alkaline solutions) to create like-charges on the particle and wafer surface, leading to electrostatic repulsion (Zeta Potential manipulation).
  Complexation: Using chelating agents to capture and remove metallic ions.

3.Post-CMP Clean for Dielectric

TEOS (Silicon Dioxide - SiO_2):
-Primary Contaminant: Slurry particles (Silica or Ceria).
-Challenge: Strong adhesion of Ceria particles via Ce-O-Si chemical bonds.
-Cleaning Strategy:
  Typically uses dilute alkaline chemistries (e.g., Ammonium Hydroxide - NH_4OH).
  This raises the pH, inducing a strong negative charge on both the TEOS surface and silica particles, promoting repulsion.
  Requires specific additives for effective Ceria removal.

SiN (Silicon Nitride):
-Primary Contaminant: Slurry particles.
-Challenge: Surface chemistry is different from oxide; can be more susceptible to particle adhesion at certain pH levels and prone to hydrolysis.
-Cleaning Strategy:
Often requires tailored chemistries or a two-step clean process.
Careful pH control is critical to avoid damaging the SiN film while ensuring efficient particle removal.

4.Post-CMP Clean for Metals

Copper (Cu):
-Primary Contaminants: Alumina/Silica particles, organic BTA residue, Cu ions.
-Challenges:
High susceptibility to corrosion and oxidation.
Galvanic corrosion when in contact with barrier metals (e.g., Ta/TaN).
Stubborn BTA (benzotriazole) residue must be removed.
-Cleaning Strategy:
Typically uses dilute acidic chemistries (e.g., citric acid, oxalic acid).
Acids help dissolve metal oxides and complex free copper ions.
Includes specific agents to strip BTA without initiating corrosion.

Tungsten (W) & Molybdenum (Mo):
-Primary Contaminants: Slurry particles, metallic residues, and oxides.
-Challenges: Avoiding galvanic corrosion and over-etching of the metal lines.
-Cleaning Strategy:
Can involve both acidic and alkaline steps.
Often utilizes oxidizing agents (e.g., H_2O_2) to form a soluble oxide layer that is then easily removed.

5.Summary & Q&A

Recap of Key Concepts:
-Cleaning must be tailored to the specific material being processed.
-Controlling surface charge (Zeta Potential) is fundamental to particle removal.
-Metal cleaning is a delicate balance between removing contamination and preventing corrosion.

METROLOGY AND INSPECTION FOR HETEROGENEOUS INTEGRATION

Taegon Kim

Hanyang University, Korea

In the age of AI, there is a constant demand to make semiconductor chips perform better. We are doing this in two main ways. The first is by making the components on the chip smaller using technologies like EUV lithography. The second, and increasingly important way, is through advanced packaging. This involves stacking different types of chips together to create one powerful and versatile device. This stacking method is known as heterogeneous integration.

A key technology for stacking these chips is Hybrid Copper Bonding (HCB). For HCB to work properly, the connections between the stacked chips must be nearly perfect. Two especially important processes here are Chemical Mechanical Planarization (CMP) and keeping the bonding process free of tiny particles. The CMP step is critical because it prepares the surface for bonding. This involves precisely controlling the topography of the tiny copper pads, particularly the dishing, where the center of the pad dips slightly. This level of precise control is absolutely essential for achieving a strong, reliable bond. At the same time, we must control dust particles, as they can get trapped during bonding and create empty spaces called voids, which can cause the final device to fail.

Because of this, the two most important quality checks for heterogeneous integration are measuring and controlling the Cu pad dishing and inspecting for voids. This tutorial will provide a clear overview of the measurement and inspection techniques used for HCB. We will focus on the latest methods to precisely manage Cu pad dishing and to find hidden voids without damaging the chip. We will discuss the main challenges involved and the solutions that are making the next generation of advanced chips possible.